IN THE CLAIMS:

1. A method of fabricating a semiconductor integrated circuit device, comprising: ~~the steps of:~~

(a) performing respective ~~a~~ wafer ~~process~~processes to ~~a plurality of wafers~~first and second wafer sets, thereby forming a plurality of semiconductor integrated circuit devices ~~over~~ on each of the wafers;

(b) after ~~step~~ operation (a), performing a first electrical test with a first test program to the first wafer set ~~to a first set of wafers selected from the plurality of wafers~~ accommodated in a first wafer cassette placed in a wafer prober; and

(c) after ~~step (a)~~operation (b), performing a second electrical test with a second test program to ~~a second set of wafers selected from the plurality of wafers~~the second wafer set accommodated in a second wafer cassette placed in the wafer prober by automatically changing ~~a test object to the second set of wafers~~a test program from the first test program to the second test program.

2. - 9. (Canceled)

10. (New) A method as claimed in claim 1, comprising:

during operation (b), performing the first electrical test to the first wafer set with first test parameters; and

during operation (c), performing the second electrical test to the second wafer set with second test parameters, by automatically changing test parameters from the first test parameters to the second test parameters.

11. (New) A method as claimed in claim 1, comprising:

during operation (b), performing the first electrical test to the first wafer set with a first prober jig configuration; and

during operation (c), performing the second electrical test to the second wafer set with a second prober jig configuration, by automatically changing the prober jig configuration from the first prober jig configuration to the second prober jig configuration.

12. (New) A method as claimed in claim 1, comprising:

performing respective wafer processes to a third wafer set, thereby forming a plurality of semiconductor integrated circuit devices on at least one wafer;

performing a third electrical test with a third test program to the third wafer set accommodated in one of the first wafer cassette and second wafer cassette, by automatically changing a test program to the third test program from a prior test program to facilitate the third electrical test.

13. (New) A method as claimed in claim 12, comprising:

performing the third electrical test to the third wafer set with third test parameters, by automatically changing test parameters from prior test parameters to the third test parameters.

14. (New) A method of fabricating a semiconductor integrated circuit device, comprising:

(a) performing respective wafer processes to first and second wafer sets, thereby forming a plurality of semiconductor integrated circuit devices on each of the wafers;

(b) after operation (a), performing a first electrical test with a first test program to the first wafer set accommodated in a first wafer cassette placed in a wafer prober; and

(c) after operation (b), performing a second electrical test with a second test program to the second wafer set accommodated in the first wafer cassette placed in the wafer prober by automatically changing a test program from the first test program to the second test program.

15. (New) A method as claimed in claim 14, comprising:

during operation (b), performing the first electrical test to the first wafer set with first test parameters; and

during operation (c), performing the second electrical test to the second wafer set with second test parameters, by automatically changing test parameters from the first test parameters to the second test parameters.

16. (New) A method as claimed in claim 14, comprising:

during operation (b), performing the first electrical test to the first wafer set with a first prober jig configuration; and

during operation (c), performing the second electrical test to the second wafer set with a second prober jig configuration, by automatically changing the prober jig configuration from the first prober jig configuration to the second prober jig configuration.

17. (New) A method as claimed in claim 14, comprising:

performing respective wafer processes to a third wafer set, thereby forming a plurality of semiconductor integrated circuit devices on at least one wafer;

performing a third electrical test with a third test program to the third wafer set accommodated in one of the first wafer cassette and a second wafer cassette, by automatically changing a test program from a prior test program to the third test program to facilitate the third electrical test.

18. (New) A method as claimed in claim 17, comprising:

performing the third electrical test to the third wafer set with third test parameters, by automatically changing test parameters from prior test parameters to the third test parameters.